FIG. 1

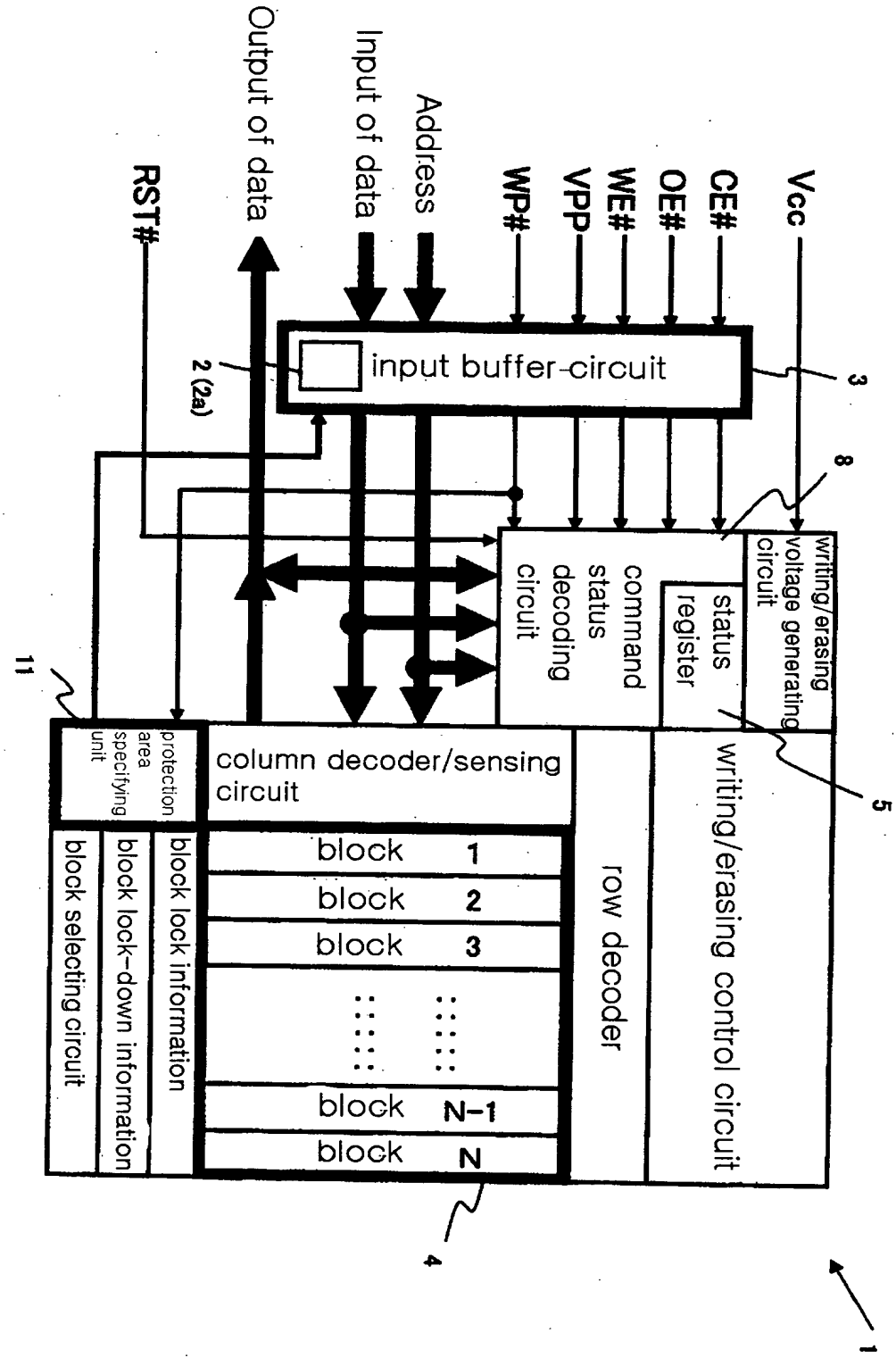

Output of data
Input of data
Address
RST#
WP#
VPP
WE#
OE#
CE#
Vcc
input buffer-circuit
2 (2a)
3
8
writing/erasing voltage generating circuit
command status decoding circuit
status register
writing/erasing control circuit
5
11
protection area specifying unit
column decoder/sensing circuit
row decoder
block 1
block 2
block 3
block N-1
block N
block lock information
block lock-down information
block selecting circuit
4
1

FIG. 2

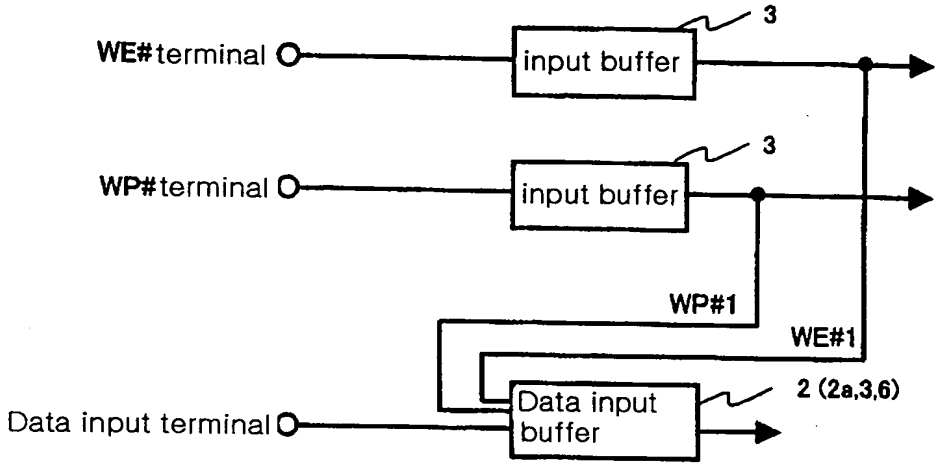

WE# terminal
input buffer
3
WP# terminal
input buffer
3
WP#1
WE#1
Data input terminal
Data input buffer
2 (2a,3,6)

FIG. 3

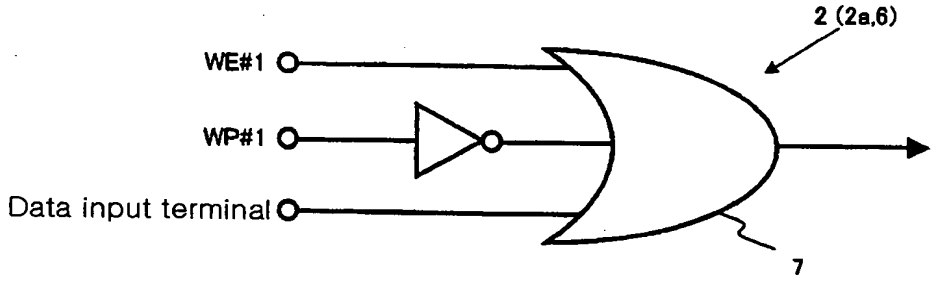

2 (2a,6)
WE#1
WP#1
Data input terminal
7

FIG. 4

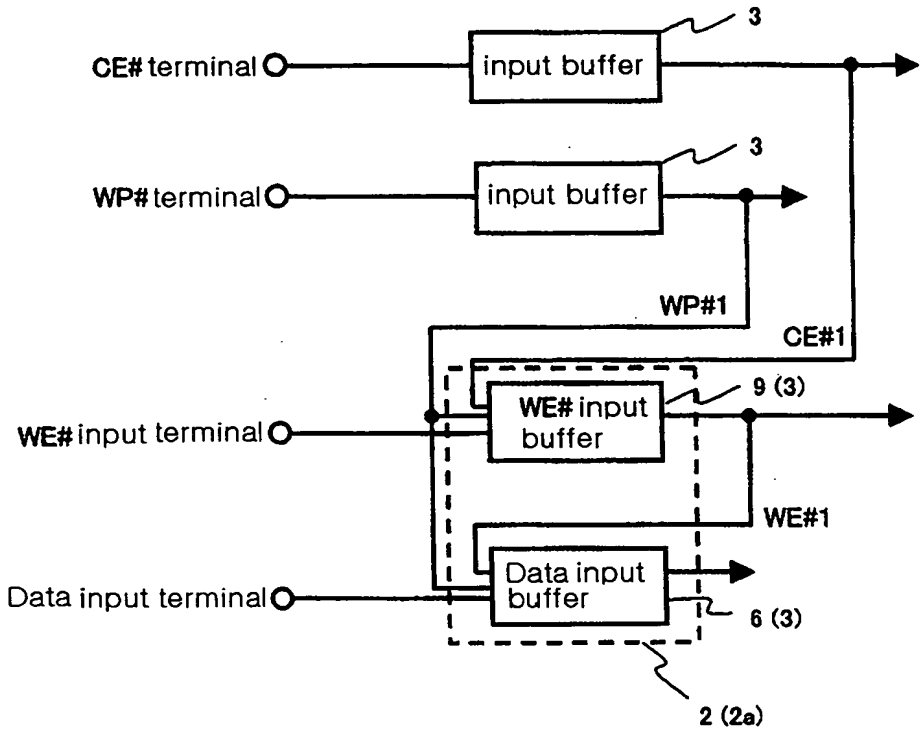

3
CE# terminal
input buffer
3
WP# terminal
input buffer
WP#1
CE#1
9 (3)
WE# input terminal
WE# input buffer
WE#1
Data input terminal
Data input buffer
6 (3)
2 (2a)

FIG. 5

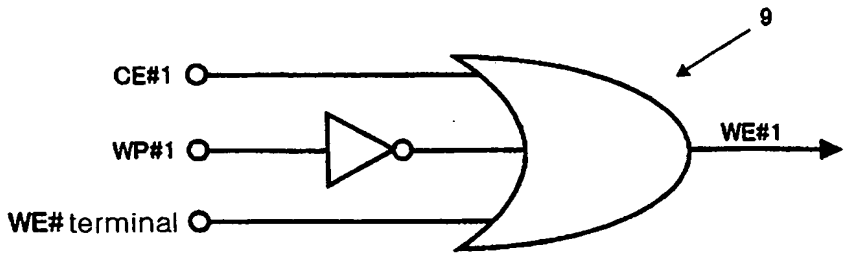

9
CE#1
WP#1
WE# terminal
WE#1

FIG. 6

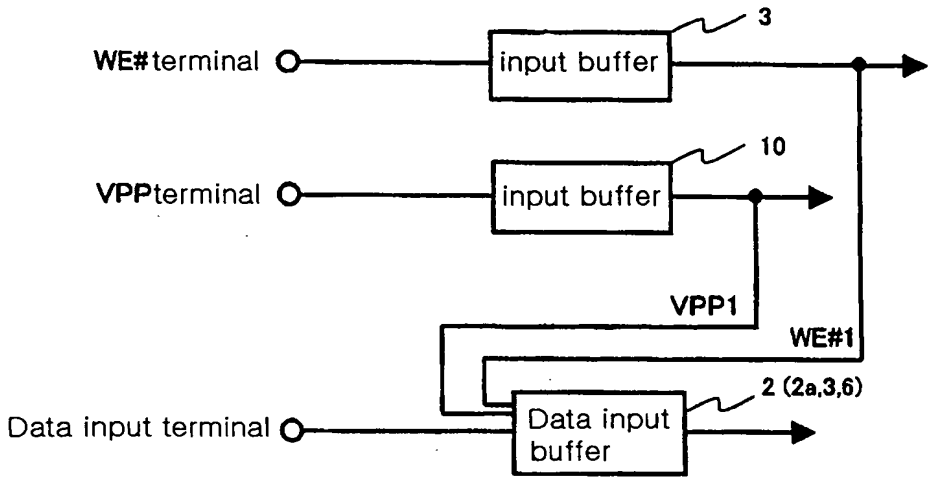

WE# terminal
input buffer
3
VPP terminal
input buffer
10
VPP1
WE#1
Data input terminal
Data input buffer
2 (2a,3,6)

FIG. 7

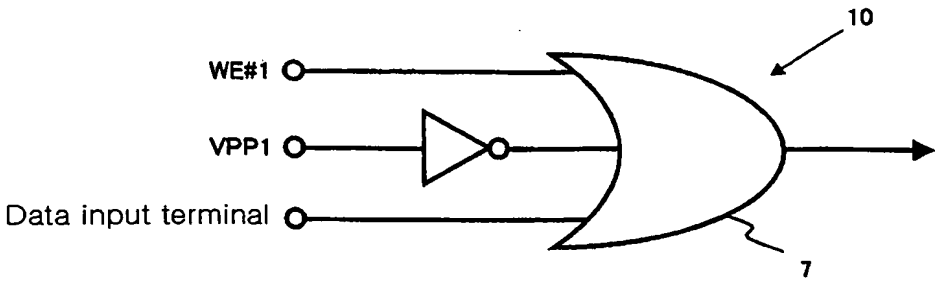

10
WE#1
VPP1
Data input terminal
7

FIG. 8

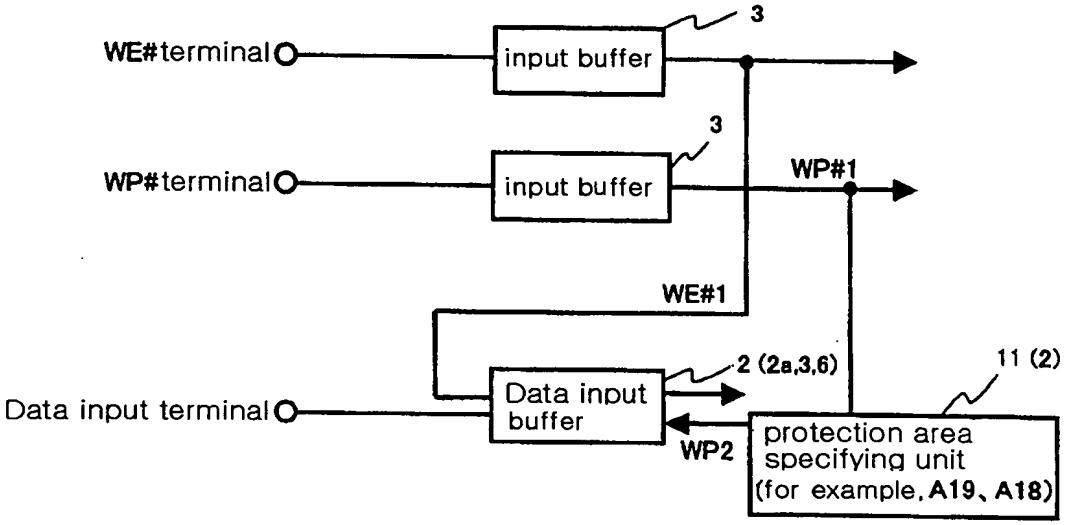

WE#terminal
input buffer
3
WP#terminal
input buffer
3
WP#1
WE#1
2 (2a,3,6)
11 (2)
Data input terminal
Data input buffer
WP2
protection area specifying unit
(for example, A19、A18)

FIG. 9

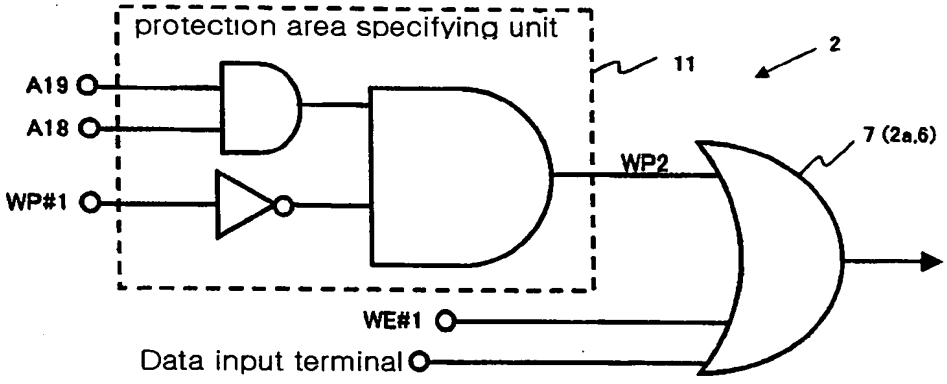

protection area specifying unit
11
2
A19
A18
WP#1
WP2
7 (2a,6)
WE#1
Data input terminal

FIG. 10

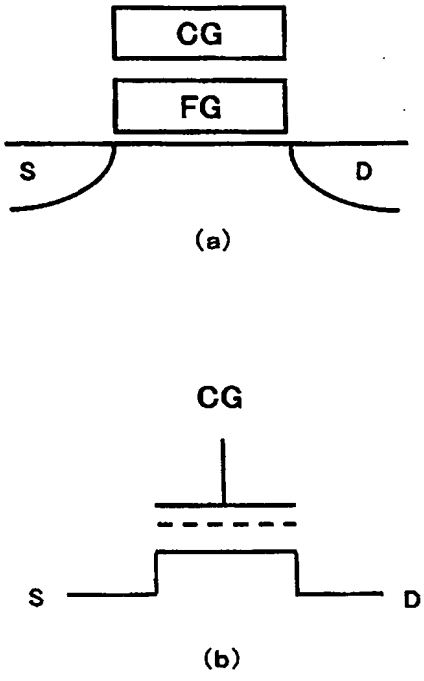
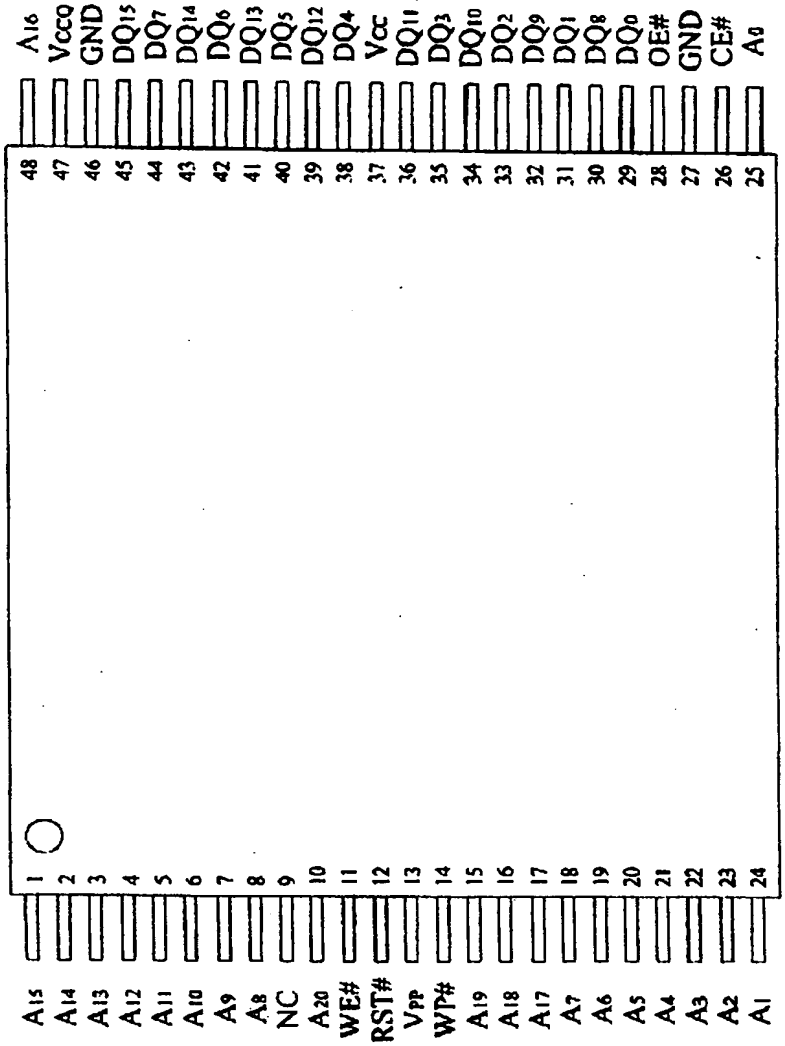


FIG. 11


A16 VCCQ GND DQ15 DQ7 DQ14 DQ6 DQ13 DQ5 DQ12 DQ4 VCC DQ11 DQ3 DQ10 DQ2 DQ9 DQ1 DQ8 DQ0 OE# GND CE# A0
48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
A15 A14 A13 A12 A11 A10 A9 A8 NC A20 WE# RST# VPP WP# A19 A18 A17 A7 A6 A5 A4 A3 A2 A1